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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	PAPER NUMBER
2121	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/883,836	BAILEY ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINE

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22, 24-36 were examined.

Section I: Final Office Action

Claim Rejections - 35 USC § 103

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5 and 7,9-14, 18, 20,21, 24, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden et al., (US Patent 5,119,483 (1992)) (hereafter Madden) in view of Peterson et al., (US Patent 6,983,237 (2006)) (hereafter Peterson) and in further view of Ravichandran (US Patent 5,966,537 (1999)). Madden, Peterson and Ravichandran are analogous arts since each one teaches electronic devices.

Per claims 1, 3, 5 and 7 Madden teaches

- identifying state information ("its mere existence" column 18, lines 24-25)
- receiving the state information (its existence prior to being simulated column 18, lines 24-25) from the first simulation model

but Madden fails to teach transferring simulation models as well as not simulating the transfer of simulation data to which Peterson and Ravichandran teach

Per claims 1 and 2 8, 9, 11, 20, 21 Peterson teaches

- comprising a transfer from a first simulation model (output of the first simulation operation into the second simulation operation, abstract, lines 1-12) in a simulation environment, said transfer being directed to a second simulation model in a circuit design being simulation in the simulation environment; and making the state information available to the second simulation model (output of

the first simulation operation into the second simulation operation, abstract, lines 1-12)

- the simulation environment comprises a plurality of simulation domains, (simulation environment defined within the disclosure as transferring state information between equivalent models...of the simulation environment [pg.22, lines 8-9] to which Peterson states transferring interaction between first and second simulation operations within the model, abstract, lines 1-12)

Per claims 1 and 8 Ravichandran teaches

- without simulating the transfer (column 6, lines 39-41 "the simulation instructions will not be executed...") in the circuit design.
- a performance for the circuit design being simulated is dynamically modified (column 2, lines 30-33) as the state information is received and made available.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Madden in view of Peterson and Ravichandran because Peterson teaches a method that allows a modeler to view one or more parameters that are linked either in a predefined-manner for automatic linkage or that are linked manually by a modeler who copies experimental results for a preceding experiment for utilization (column 4, line 61-64). Ravichandran teaches a dynamic

optimizing compiler, which uses input data to profile a computer application in systematic manner suitable for producing a highly optimized executable (column 2, lines 30-34).

Per claims 2, 4 and 7 Peterson teaches

- transferring at least one additional simulation model (i.e., third simulation operation, columns 11 and 12, lines 7-11 and 1-2, respectively) in the simulation environment.

Per claims 3,4 and 7 Ravichandran teaches

- a coherent state memory space that is part of the simulation environment and corresponds to an element in the circuit design being simulated, said coherent state (using the results of a previous computation for re-calculation: abstract, lines 14-15)
- memory spaces, (column 4, lines 40-42); storing the additional state information (stores state table: columns: 6, lines 60-65)

Per claim 5 Ravichandran teaches

- at least one of a virtual transfer path for use when a simulation model of a transfer path in the circuit design is not included in the simulation environment (transfer between original vectors and optimization vectors which appears separate from simulation event: column 8, lines 25-27); and a higher

performance transfer path than the simulation model of the transfer path in the circuit design (path continues if changes pass optimization metric, if smaller, the optimization is completed, if not, more interactions continue: column 8, lines 8-24).

Per claim 9 Ravichandran teaches

- a software execution domain, (column 1, lines 29-30) a hardware (column 1, lines 43; column 2, lines 41-42)

Per claim 11 Ravichandran teaches

- at least one of a logic (column 1, lines 43; column 2, lines 41-42) simulator and a programming language (column 4, line 4) simulator.

Per claim 12 Ravichandran teaches

- the logic simulator comprises one of a hardware description language (HDL) ("C" and "C++" are examples of gate-level programming languages: column 4, lines 2-4)

Per claim 13, Ravichandran teaches

- simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, (column 4, lines 2-4) a simulator using a C-

based language, a simulator using a C++ based language, and a JAVA (column 1, lines 29-30) programming language simulator.

Per claim 14, Ravichandran teaches

- one simulation model of a circuit element in the circuit design (e.g., microprocessors: column 10, lines 20-23).

Per claim 18, Ravichandran teaches

- a programming language (column 4, line 4)

Per claim 21, Ravichandran teaches

- advancing simulation time only in each activated simulation domain (suggestion of discriminating instructions: column 6, lines 39-41).

Per claim 24 Ravichandran teaches

- the system state comprises system addresses (column 5, lines 15-28) in the circuit design.

Per claim 30 Peterson teaches

- both the first simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) and the second simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) are within a same simulation domain (i.e., simulation model using the first and second simulation operations, abstract, lines 1-12) in the simulation environment.

Per claim 31 Peterson teaches

- the first simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) and the second simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) (i.e., simulation model using the first, second and third simulation operation, columns 11 and 12, lines 7-11, 1-10, respectively) is in the simulation environment.

4. Claims 6, 8-10,12,14-16,18-22,24-29,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden, in view of Peterson and Ravichandran and further in view of Bailey et al., ("Hardware/Software Co-Simulation Strategies for the Future" (February 2000)). Madden as modified by Peterson and Ravichandran recited in claims

1 and 8 for the reasons above differing from the invention as recited in claims 6, 8-10,12,14-16,18-22,24-29,31 in their combined teaching lacks.

Per claim 6 Bailey teaches

- the higher performance transfer path (pg. 6, Accuracy paragraph, lines 7-9) provides a lower level of resolution (pg. 6, cycle section, lines 1-3) than the simulation model of the transfer path in the circuit design.

Per claims 8 and 21 Bailey teaches

- the method comprising: selectively activating and deactivating (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4) particular simulation domains in the simulation environment such that a resolution (pg. 6, cycle section, lines 1-3)

Per claim 9 Bailey teaches

- an abstract (suggestion of a level of abstraction; pg.4, Bus Functional Model, lines 7-8) model simulation domain.

Per claim 10 Bailey teaches

- least one of a native processor package, an instruction set simulator (ISS), (suggestion of a level of an instruction set; pg.4, Bus Functional Model, lines 7-8) and a programming language simulator to model software execution in one or more processors (mention of software execution; pg. 3, 3rd paragraph, lines 4-6).

Per claim 12, Bailey teaches

- based simulator, a gate-level simulator (pg. 6, Performance section, lines 4-7), a simulation accelerator (pg. 6, Performance section, lines 6-7), a system simulator, a cycle simulator (pg. 6, Cycle section), and a programmable hardware emulator (pg. 6, Emulation section).

Per claims 14 and 18 Bailey teaches

- the hardware simulation domain (pg. 1, abstract, lines 7-9)

Per claim 15, Bailey teaches

- partitioning the circuit design (pg. 2, 4th paragraph, lines 6-7) into the plurality of simulation domains (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1| based on a partition criteria (pg. 2, 4th paragraph, lines 6-7).

- partitioning the circuit design based on the abstraction level (suggestion of a level of abstraction; pg.4, Bus Functional Model, lines 7-8) partition the circuit deign into at least one of a pin-level domain (pg. 5, Instruction Set Simulation section, lines 1-2), a bus-level domain (suggestion of function type; pg. 7, 4th paragraph), and a transaction-level domain.

Per claim 16, Bailey teaches

- the partition criteria (pg. 2, 4th paragraph, lines 6-7) comprises at least one of an abstraction level, (suggestion of a level of abstraction; pg.4, Bus Functional Model, lines 7-8) a simulation type, and a function type (suggestion of function type; pg. 7, 4th paragraph).

Per claim 18, Bailey teaches

- partitioning (pg. 2, 4th paragraph, lines 6-7) the circuit design based on the simulation type partitions the circuit design into at least one of a software execution domain (pg. 4, paragraphs 4-7), a logic simulator domain,

Per claim 19 Bailey teaches

- partitioning the circuit design based on the function type comprises (suggestion of function type; pg. 7, 4th paragraph): identifying one or more function elements in the circuit design that have a particular level (example of a high-level; pg. 5,

lines3-5) of independent operation from the remainder of the circuit design; and defining of a domain (suggestion of domains; pg.7, 4th paragraph) encompassing each identified functional element.

Per claim 20 Bailey teaches

- the particular simulation domains are selectively activated or deactivated (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4) during particular stages of simulation in combinations that either accelerate performance (pg. 6, Performance section, lines 5-7) of the simulation environment or increase resolution of the simulation environment.

Per claims 22 and 25 Bailey teaches

- the plurality of simulation domains (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) are to be active for the identified system state comprises at least one of a centralized control, a transaction-based control, (pg. 6, cycle section, lines 3-4) and a distributed control.

Per claim 25, Bailey teaches

- active for the data transaction (pg. 6, cycle section, lines 3-4), and wherein the transaction-based control comprises: sending a message to a centralized simulation clock as part of the data transaction (pg. 6, cycle section, lines 3-4),

said message to instruct the centralized simulation clock with respect to which of the plurality of simulation domains are to be active for the data transaction (pg. 6, cycle section, lines 3-4).

Per claim 26, Bailey teaches

- predetermined simulation domain (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) is configured with activation information identifying at least one particular system state for which the predetermined simulation domain is to be active (section teaches whether to reduce or eliminate all further occurrences; pg. 6, Accuracy Section, lines 6-9), wherein identifying the system state comprises receiving a broadcast of the system state at the predetermined simulation domain comprises determining if the predetermined simulation domain is to be active for the identifying system state based on the activation information (cycle state discloses scheduling timing details, i.e., current state of inputs; pg. 6, 2nd paragraph); and advancing an operation in the predetermined simulation domain according.

Per claim 27, Bailey teaches

- the information further identifies an event for terminating operation (pg. 7, Cross-Domain Optimization section, lines 3-5) of the predetermined simulation domain for the at least one particular system state.

Per claim 28, Bailey teaches

- plurality of simulation domains (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) are to be active for the identified system state depends on a plurality of control mechanisms, wherein each of the plurality of control mechanisms comprises a priority level, and wherein a higher priority control mechanism takes precedence over a lower priority control mechanism (section discusses the importance of higher performance levels, thus describing priority; Accuracy Section, lines 3-9).

Per claim 29, Bailey teaches

- the plurality of simulation domains (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) comprises a hierarchical structure and wherein selectively activating and deactivating (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4) the particular simulation domains(simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) is based on levels of the hierarchical structure.

Per claim 31, Bailey teaches

- different simulation domains(simulation domains; pg. 1, Abstract, lines 8-9 and figure 1)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Madden in view of Peterson and Ravichandran

with Bailey because Bailey teaches an improved test and integration phase to improve the risk levels associated with on-time delivery (pg. 3, 6th paragraph, lines 1-2).

5. Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden (US Patent 5,119,483 (1992)) in view of Peterson (US Patent 6,983,237 (2006)) and in further view of Bailey.

Per claims 32, 35 and 36 Madden teaches

- identifying state information (its mere existence column 18, lines 24-25)
- receiving the state information (its existence prior to being simulated column 18, lines 24-25) from the first simulation model

but Madden fails to teach a first and second simulations in simulation environment and deactivating a simulation engine to which Peterson and Bailey teach, respectively.

Per claim 32 Peterson teaches

- a first simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) in a simulation environment when a simulation domain of the first simulation model (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5)

- the simulation environment prior to activation of a simulation domain of the second simulation model, (abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5) said first simulation model (column 10, lines 33-44) and said second simulation model (column 10, lines 33-44) representing different version (e.g., changing a resistor on a board, design choice or a third simulation operation, columns 11-12, lines 7-11, 1-10, respectively) of a same functionality in a circuit design being simulation.

Per claim 32 Bailey teaches

- deactivated (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Madden in view of Peterson and Bailey because Peterson teaches a method that allows a modeler to view one or more parameters that are linked either in a predefined-manner for automatic linkage or that are linked manually by a modeler who copies experimental results for a preceding experiment for utilization (column 4, line 61-64). Bailey teaches an improved test and integration phase to improve the risk levels associated with on-time delivery (pg. 3, 6th paragraph, lines 1-2).

Per claim 33 Peterson teaches

- the first simulation model (column 10, lines 33-44)and the second simulation model (column 10, lines 33-44) each have a particular level of performance and resolution, and wherein simulation of the circuit design switches from the first simulation model (column 10, lines 33-44) to the second simulation model (column 10, lines 33-44) is based on a change in a performance level and/or a resolution level desired at a difference stage of simulation.

Per claim 34 Peterson teaches

- first simulation model (column 10, lines 33-44) and the second simulation model (column 10, lines 33-44) are among a plurality of simulation models (abstract: lines 1-12 "first and second") representing a same functionality in the circuit design, each of the plurality of simulation models (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) having a particular level of performance and resolution, and each of the plurality of simulation models (simulation domains; pg. 1, Abstract, lines 8-9 and figure 1) being used at different stages of simulation depending on a desired performance level and/or resolution level of the simulation.

Per claim 35 Bailey teaches

- A machine readable medium having stored thereon machine executable instructions (pg. 5, Instruction Set Simulation, 1st paragraph) that when executed implement

Per claim 35 Peterson teaches

- a method comprising: identifying state information comprising a transfer from a first simulation model (simulation environment defined within the disclosure as transferring state information between equivalent models...of the simulation environment [pg.22, lines 8-9] to which Peterson states transferring interaction between first and second simulation operations within the model, abstract, lines 1-12)
- in a simulation environment, said transfer being directed to a second simulation model (simulation environment defined within the disclosure as transferring state information between equivalent models...of the simulation environment [pg.22, lines 8-9] to which Peterson states transferring interaction between first and second simulation operations within the model, abstract, lines 1-12) in a circuit design being simulation environment;

- the first simulation model (column 10, lines 33-44); and making the state information available to the second simulation model without simulating the transfer(simulation environment defined within the disclosure as transferring state information between equivalent models...of the simulation environment [pg.22, lines 8-9] to which Peterson states "linking a sequence of experiments....Input conditions that constitute the output of a first experiment do thus not have to be restated for each of the further experiments and outputs of the experiment....A single experiment sequence, for example including experiment and experiment may be defined in a single experiment [column 5, lines 15-23]) in the circuit.

Per claim 35 Madden teaches

- receiving the state information (column 18, lines 24-25)

Per claim 36 Bailey teaches

- A machine readable medium having stored thereon machine executable instructions (pg. 5, Instruction Set Simulation, 1st paragraph)
- deactivated (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4)

Per claim 36 Madden teaches

- Reading/Writing state information (its mere existence prior to simulation column 18, lines 24-25)

Per claim 36 Peterson teaches

- from a first simulation model (column 10, lines 33-44) in a simulation environment when a simulation domain of the first simulation model (column 10, lines 33-44)

- to a second simulation model (column 10, lines 33-44) in the simulation environment prior to activation of a simulation domain of the second simulation model, said first simulation model (column 10, lines 33-44) and said second simulation model (column 10, lines 33-44) representing different versions (e.g., changing a resistor on a board, design choice or a third simulation operation, columns 11-12, lines 7-11, 1-10, respectively) of a same functionality in a circuit design being simulated.

Section II: Response to Applicants' Arguments (Previous Office Action)

Claims 1-5 and 7/ 6, 8-22 and 24-31

Applicants are thanked for addressing this issue; however the arguments are non-persuasive in view of the prior art. The source of the motivation to combine stems from the prior art as stated in each occurrence above.

In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicants are correct in stating Madden is silent to the limitations stated in applicants' arguments (pg. 10, 1st paragraph lines 4-8); however, Peterson reflects the limitations (abstract, lines 1-12).

The Office believes the Madden reference teaches the state information limitation (column 11, lines 16-21). Applicants argue that Madden fails to neither identify nor receive this limitation to which the Office claims inherency by reasoning of the state information mere existence, otherwise its properties and functions would never be utilized let alone discussed.

Paterson teaches transferring a first simulation to a second simulation as denoted in the abstract, lines 1-12 and in columns 10 and 11, lines 60-67 and 1-5, respectively, since the output of the first simulation is applied as the input of the second simulation operation.

Applicants argue that the Ravichandran fails to cure the deficiencies of a first and second simulation model to which Peterson solves. However, Ravichandran is analogous art since it does teach simulation (column 6, lines 39-41 "the simulation instructions will not be executed...").

Claims 32-36

Applicants are thanked for addressing this issue; however the arguments are non-persuasive in view of the prior art. The motivation to combine and the expectations of success are clearly denoted after each group of claims as stated above. Reading and writing state information is an inherent process by its mere existence to perform the simulation, otherwise the purpose of simulating a state machine without the computer reading or writing it is pointless.

Applicants argue Madden fails to teach nor suggest the limitations as stated in their argument on page 12, paragraph 5 to which Paterson does teach (abstract).

In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It's the combination of Madden's state information and Peterson' simulation models that anticipates the limitations stated in applicants response (pgs. 12-13, last paragraph to first paragraph, respectively).

To refute applicants' claim that Peterson fails to teach first and simulation models, the Office refers to the abstract, line 4-12, which states first and second

simulation operations that are part of the "computer-based simulation model" (abstract, lines 1-3). Furthermore, "representing different versions of the same functionality in a circuit" (applicants' response, pg.13, 3rd paragraph, lines 5-7) is a broad term in and of its self; however, an individual can simply, for example, change a resistance value, thus the design changes/choices are infinite.

The deactivation limitation is taught by Bailey deactivated (selectively suppressing activity; pg. 7, Cross-Domain Optimization section, lines 3-4). Logically, if a machine has the ability to deactivate a device, then it must have been active from the start. In response to the prima facie argument involving Madden, Peterson and Ravichandran, conversely, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ravichandran in view of Madden and Paterson because Madden teaches a method to reduce the processing time required for correcting a fault (column 3, lines 1-2). Peterson teaches a method which utilizes any one of a number of commercially available modeling tools to model a wide variety of systems (column 2, lines 46-48). Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Peterson in view of Madden and Ravichandran because Madden teaches a method to reduce the processing time required for correcting a fault (column 3, lines 1-2). Ravichandran teaches a dynamic optimizing compiler, which uses input data to profile a computer application in systematic manner suitable for producing a highly optimized executable (column 2, lines 30-34).

The Office stands behind the teaching of Peterson's first and second simulation operations as part of the simulation model to which is equivalent to the applicants' simulation domain. To add "the different versions of the these of the same functionality" were previously refuted within this section of the Office action.

The rejection, as set forth above, stands.

Request for Interview

6. The Examiner and attorney of record, Mr. Justin Wagner, discussed the limitations *(1/25/07)* in view of the Peterson reference regarding *the first simulation model in a simulation environment, said transfer being directed to a second simulation model in a circuit design being simulated in the simulation environment.* The Examiner pointed to the abstract of Peterson as well as columns 11 and 12 to argue that the prior art anticipated this limitation, thus both parties were not in agreement on this issue.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

5,870,588 A hardware and software co-design environment and design methodology based on a data-model that allows one to specify, simulate, and synthesize heterogeneous hardware and software architectures from a heterogeneous specification.

5,953,519 A method and system for generating electronic hardware simulation model segments is disclosed. The input to the method and system are abstraction models that define the mappings between the signals of electronic circuit models and the signals of specification models expressed at higher levels of temporal and/or data abstraction. Abstraction models are converted into simulation model segments using a two-step process where abstraction models are first converted into intermediate data structures. A second step converts the data structures into simulation model segments in any of the standard hardware description languages (HDLs). Useful applications of the method and system include automated simulation test bench generation and automated synthesis of hardware design models from behavioral specifications.

US 6134516 The SEmulation system provides four modes of operation: (1) Software Simulation, (2) Simulation via Hardware Acceleration, (3) In-Circuit Emulation (ICE), and (4) Post-Simulation Analysis. At a high level, the present invention may be embodied in each of the above four modes or various combinations of these modes.

US 6314552 An electronic design is created through a machine implemented method that includes evolutionarily generating candidate architectures for the electronic design, with the evolutionary generation of the candidate architectures being periodically guided by the designer, and generating an implementation specification for the design in accordance with a selected one of the evolutionarily generated candidate architectures.

US 7054802 A system is provided to increase the accessibility of registers and memories in a user's design undergoing functional verification in a hardware-assisted design verification system. A packet-based protocol is used to perform data transfer operations between a host workstation and a hardware accelerator for loading data to and unloading data from the registers and memories in a target design under verification (DUV) during logic simulation. The method and apparatus synthesizes interface logic into the DUV to provide for greater access to the registers and memories in the target DUV which is simulated with the assistance of the hardware accelerator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

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